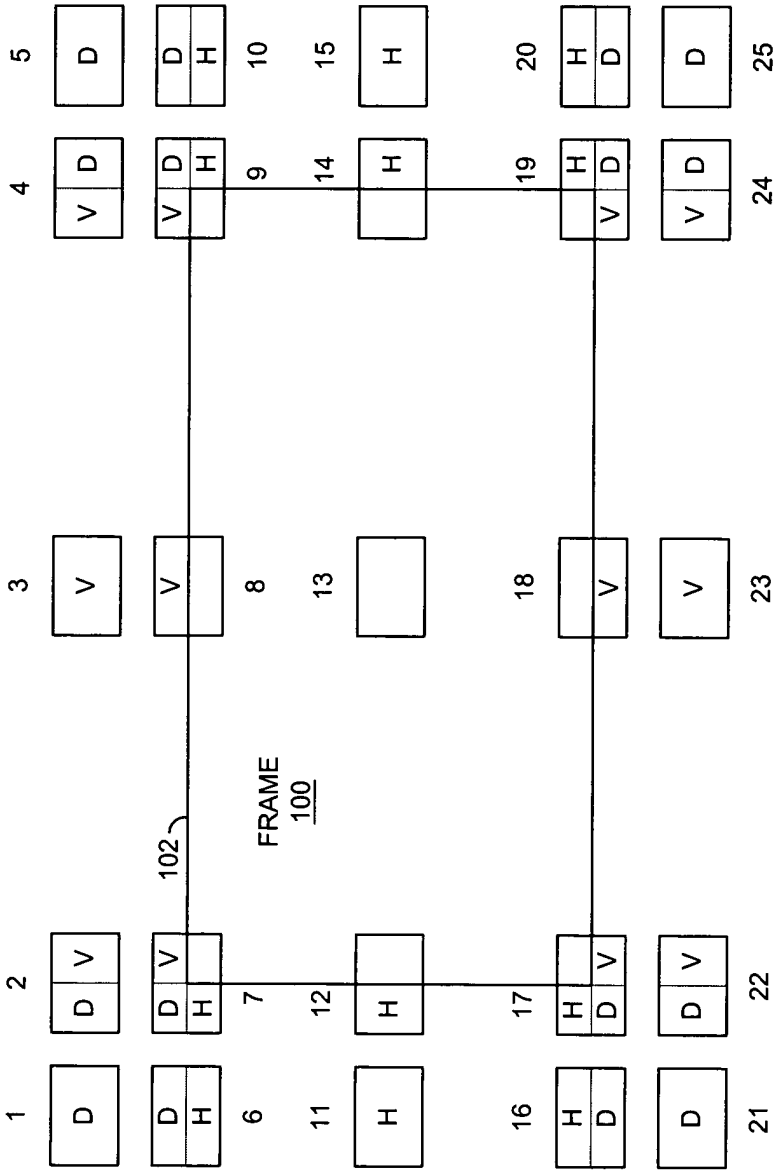
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
D
V
H
102
FRAME
100

FIG. 1

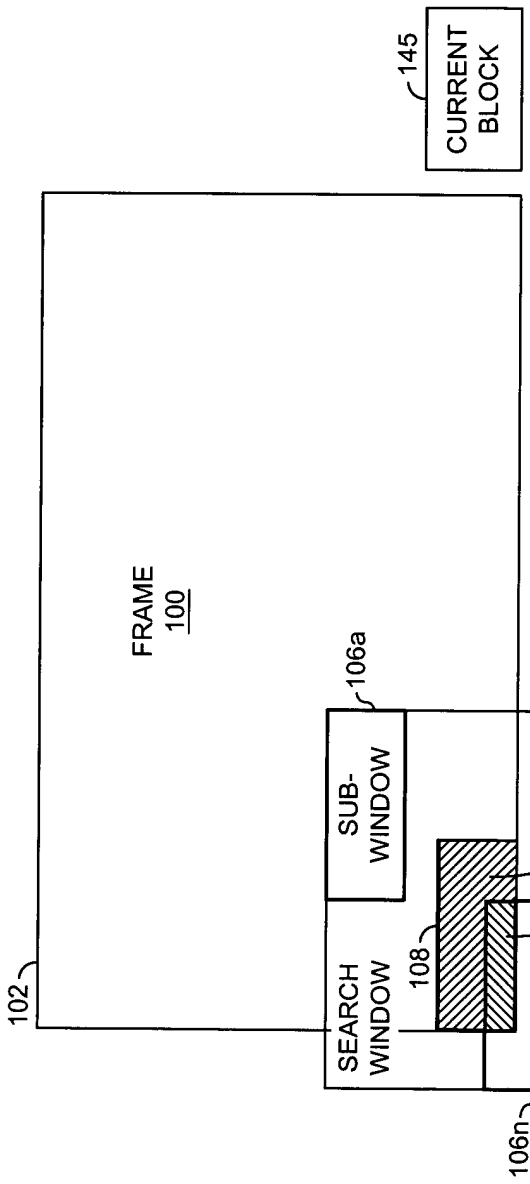
145
CURRENT BLOCK
FRAME
100
102
106a
SUB-WINDOW
104
112
110
108
SEARCH WINDOW
116
106n

FIG. 2

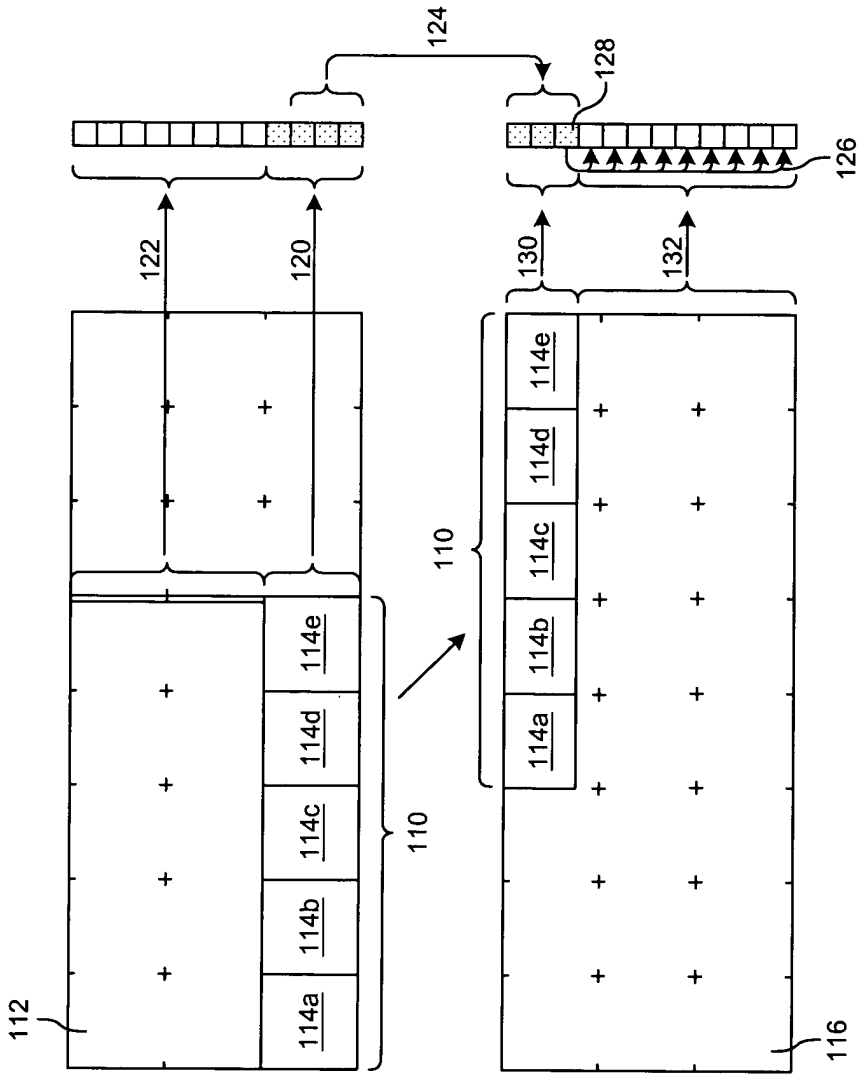
124
128
126
122
120
130
132
110
114a
114b
114c
114d
114e
112
116

FIG. 3

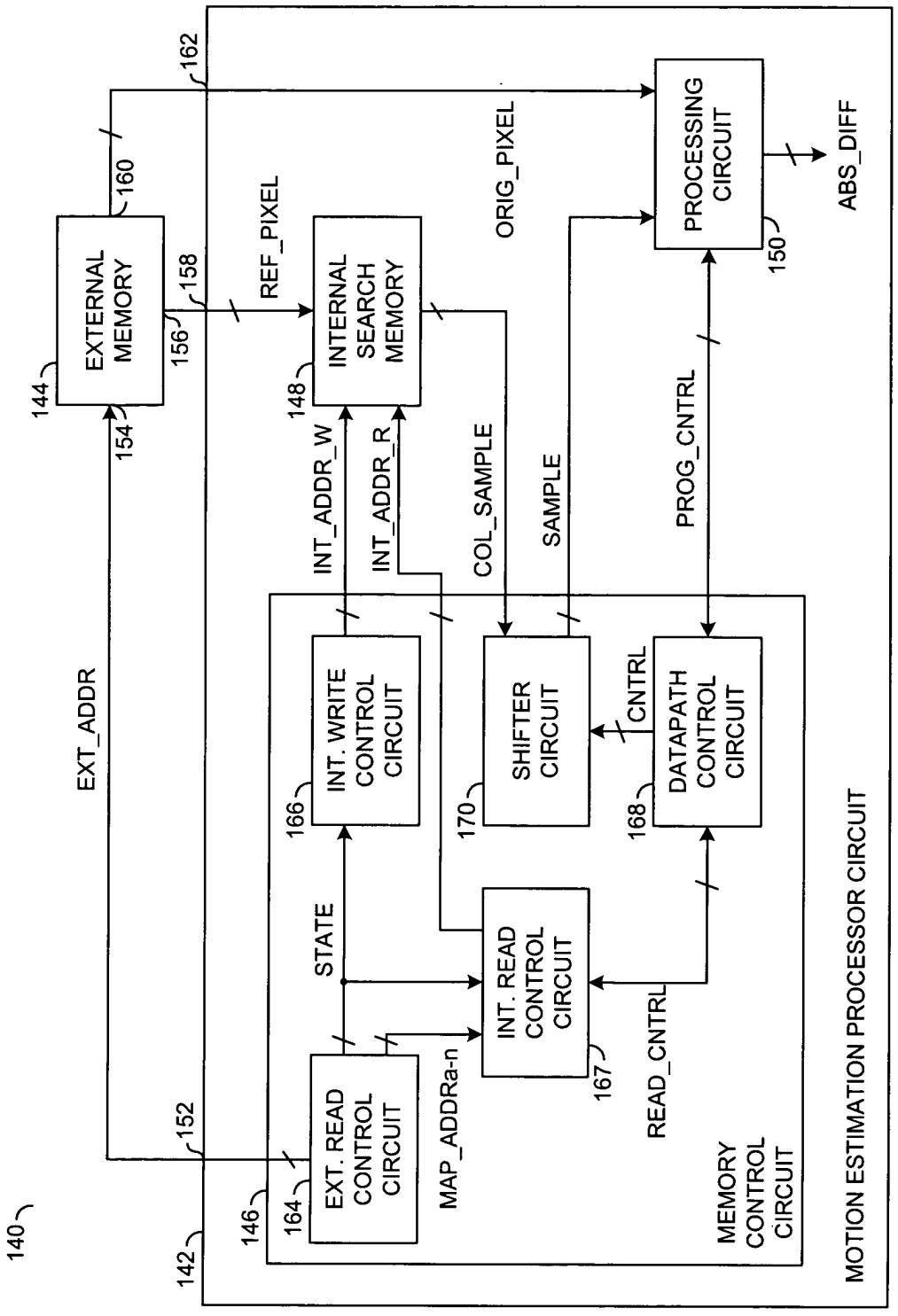
140
142
MOTION ESTIMATION PROCESSOR CIRCUIT
146
MEMORY CONTROL CIRCUIT
144
EXTERNAL MEMORY
154
156
158
160
162
EXT_ADDR
REF_PIXEL
ORIG_PIXEL
ABS_DIFF
148
INTERNAL SEARCH MEMORY
150
PROCESSING CIRCUIT
INT_ADDR_W
INT_ADDR_R
COL_SAMPLE
SAMPLE
PROG_CNTRL
152
164
EXT. READ CONTROL CIRCUIT
166
INT. WRITE CONTROL CIRCUIT
170
SHIFTER CIRCUIT
168
DATAPATH CONTROL CIRCUIT
CNTRL
STATE
MAP_ADDRa-n
167
INT. READ CONTROL CIRCUIT
READ_CNTRL

FIG. 4

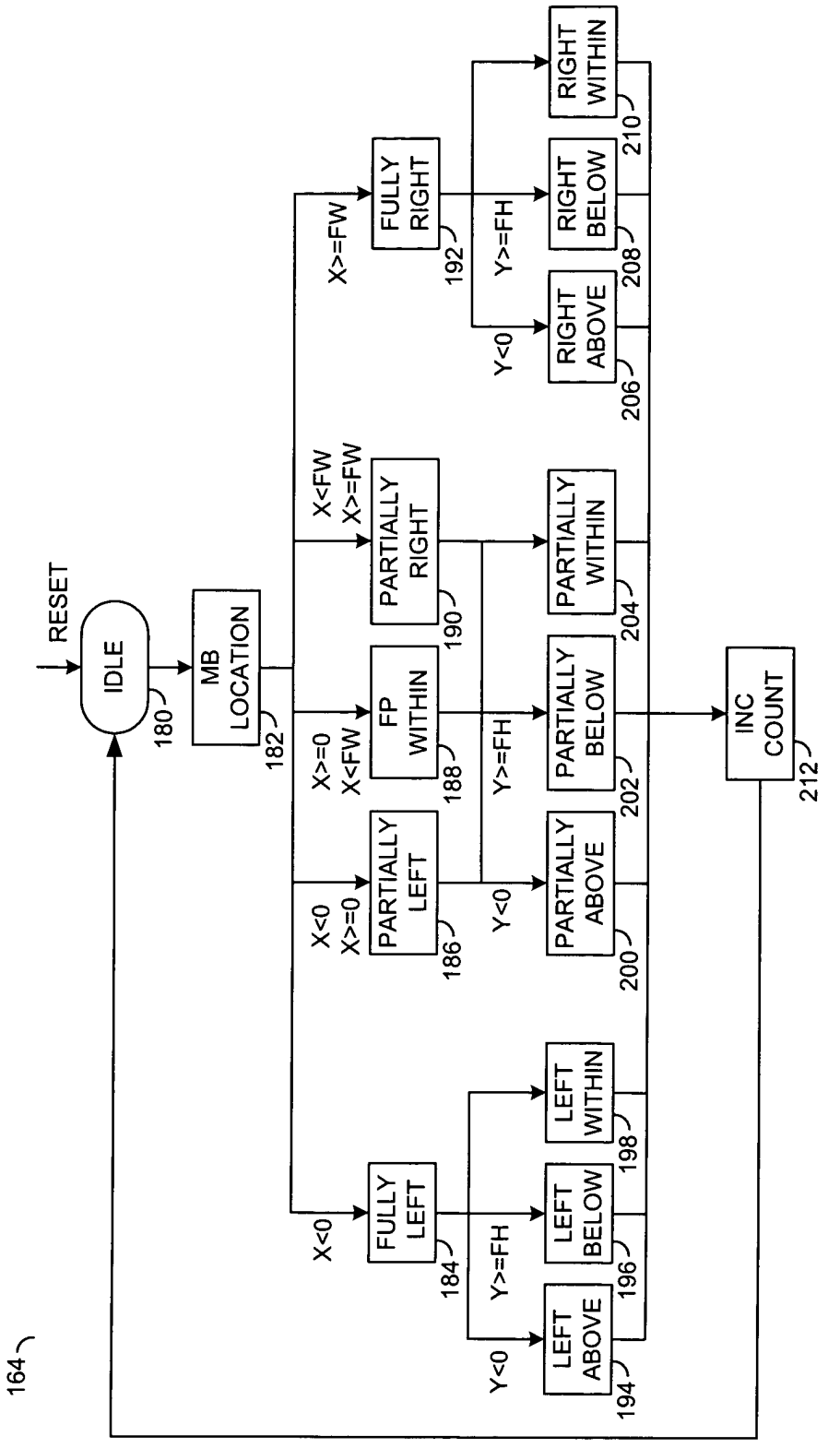
164
RESET
IDLE
180
MB LOCATION
182
X<0
X>=0
X<FW
X>=FW
X>=FW
FULLY LEFT
184
PARTIALLY LEFT
186
FP WITHIN
188
PARTIALLY RIGHT
190
FULLY RIGHT
192
Y>=FH
Y<0
Y>=FH
Y<0
Y>=FH
Y<0
LEFT ABOVE
194
LEFT BELOW
196
LEFT WITHIN
198
PARTIALLY ABOVE
200
PARTIALLY BELOW
202
PARTIALLY WITHIN
204
RIGHT ABOVE
206
RIGHT BELOW
208
RIGHT WITHIN
210
INC COUNT
212

FIG. 5

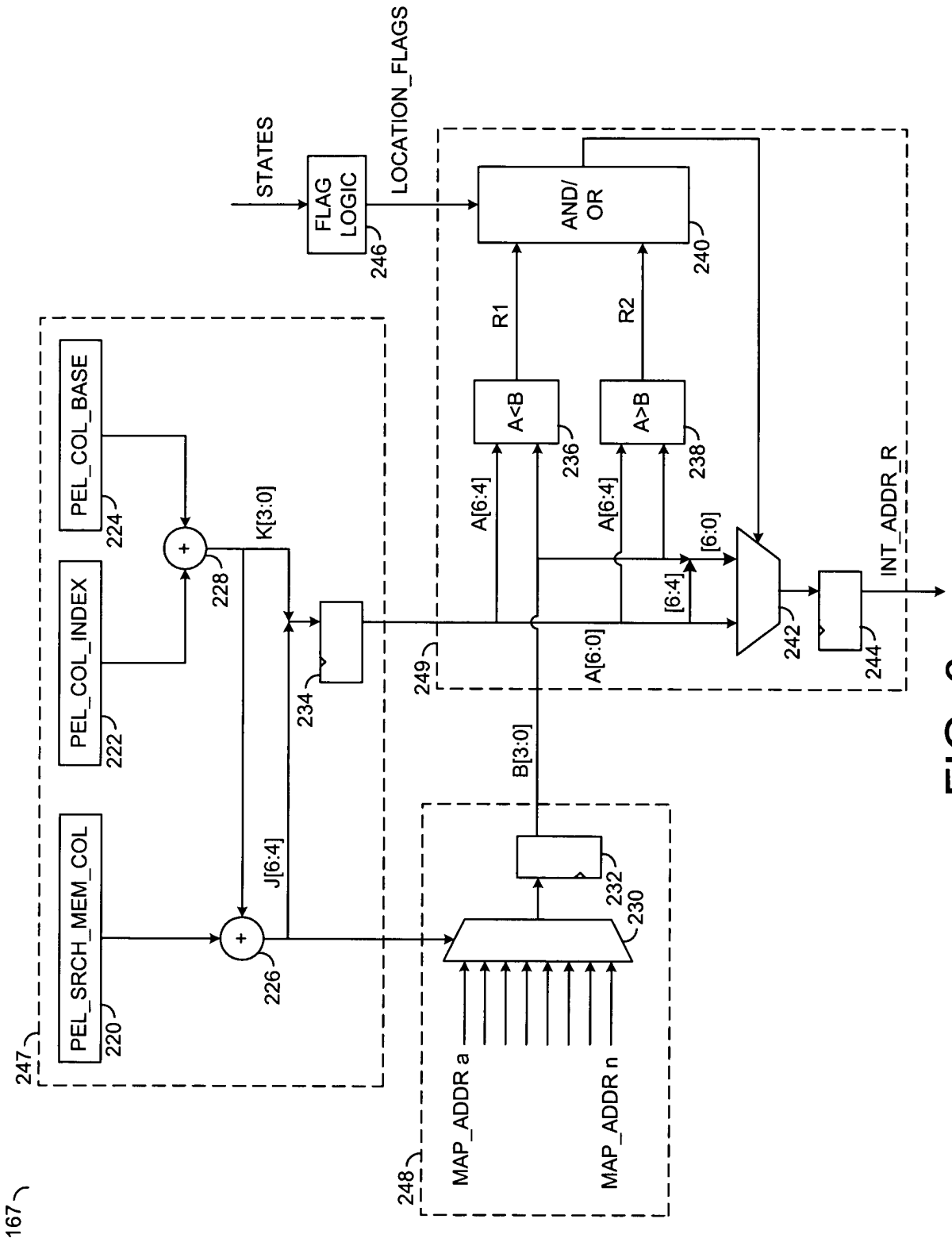
167
247
PEL_SRCH_MEM_COL
220
PEL_COL_INDEX
222
PEL_COL_BASE
224
228
K[3:0]
226
J[6:4]
234
STATES
FLAG LOGIC
246
LOCATION_FLAGS
AND/ OR
240
R1
R2
A<B
236
A>B
238
A[6:4]
A[6:4]
[6:0]
[6:4]
249
A[6:0]
242
244
INT_ADDR_R
B[3:0]
232
230
248
MAP_ADDR a
MAP_ADDR n

FIG. 6

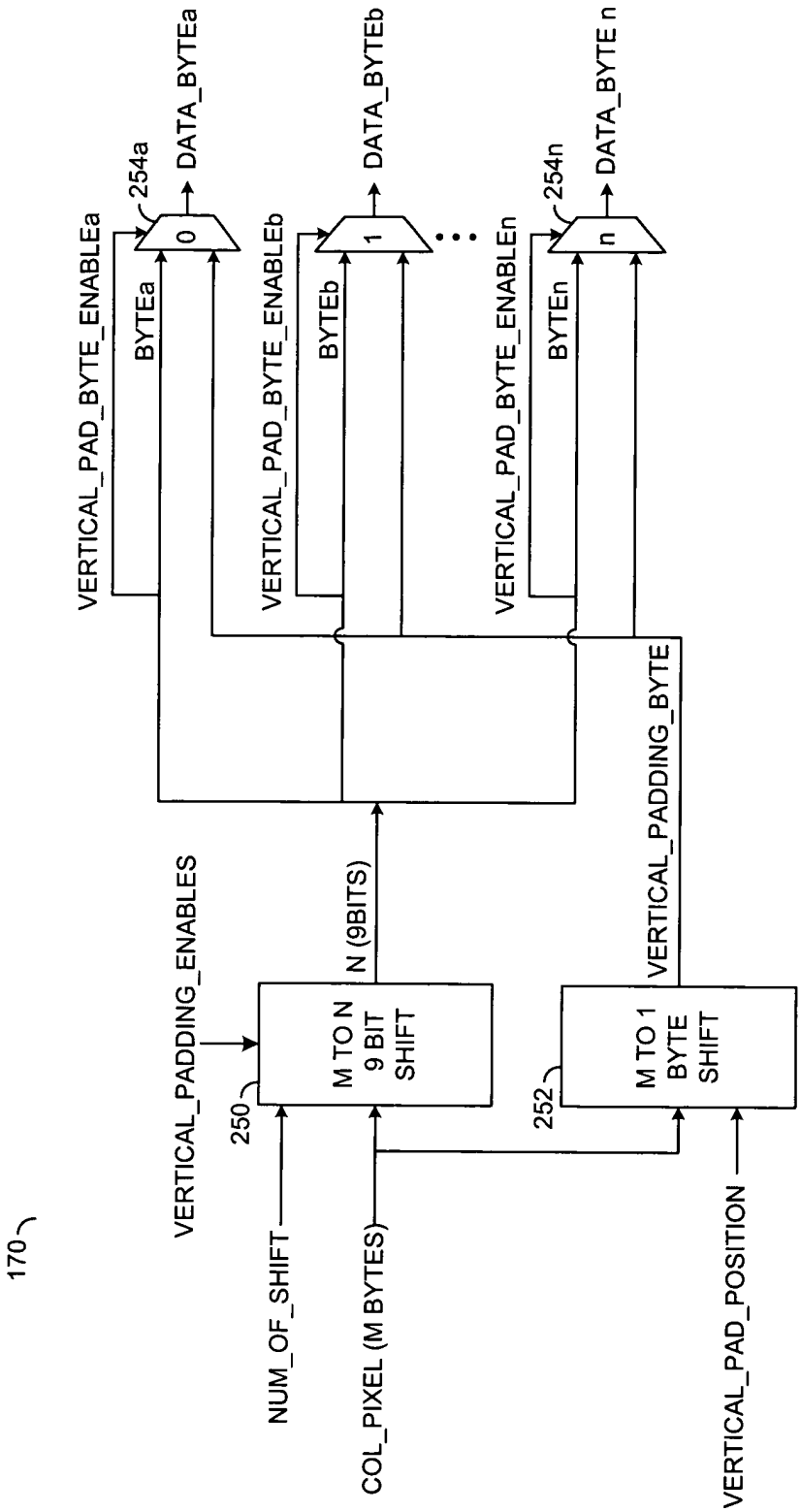
170
VERTICAL_PADDING_ENABLES
NUM_OF_SHIFT
COL_PIXEL (M BYTES)
250
M TO N
9 BIT
SHIFT
N (9BITS)
252
M TO 1
BYTE
SHIFT
VERTICAL_PADDING_BYTE
VERTICAL_PAD_BYTE_ENABLEa
BYTEa
254a
0
DATA_BYTEa
VERTICAL_PAD_BYTE_ENABLEb
BYTEb
1
DATA_BYTEb
VERTICAL_PAD_BYTE_ENABLEn
BYTEn
254n
n
DATA_BYTE n
VERTICAL_PAD_POSITION

FIG. 7